

# UM10057

## ISP1760, ISP1761 Hi-Speed USB Host/On-The-Go Demo Board for BSQUARE DevIDP PXA255

Rev. 01 — 2 May 2006

User manual

### Document information

Info	Content
<b>Keywords</b>	isp1760; isp1761; host controller; universal serial bus; otg controller; usb; otg; onthego
<b>Abstract</b>	<p>This eval board allows demonstration of the ISP176x functionality on a BSQUARE DevkitIDP for PXA255 development platform.</p> <p><b>Remark:</b> ISP176x denotes the ISP1760 and ISP1761 Hi-Speed Universal Serial Bus controllers, and any future derivatives.</p>

### Revision history

Rev	Date	Description
01	20060502	First release.

## Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, please send an email to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

**Remark:** ISP176x denotes the ISP1760 and ISP1761 Hi-Speed Universal Serial Bus Controllers, and any future derivatives.

## 1. Introduction

The ISP176x is a Hi-Speed Universal Serial Bus (USB) Controller with three USB ports. For ISP1761, which has On-The-Go (OTG), port 1 can be configured to function as a downstream port, an upstream port or an OTG port; ports 2 and 3 are always configured as downstream ports. For the ISP1760 host controller, all three ports are downstream.

The ISP176x is accessible through a generic processor interface with de-multiplexed address and data lines.

This evaluation (eval) board allows demonstration of the ISP176x functionality on a BSQUARE DevkitIDP for PXA255 development platform.

[Fig 1](#) shows the Philips ISP1760/1 add-on card for the BSQUARE DevkitIDP for PXA255.

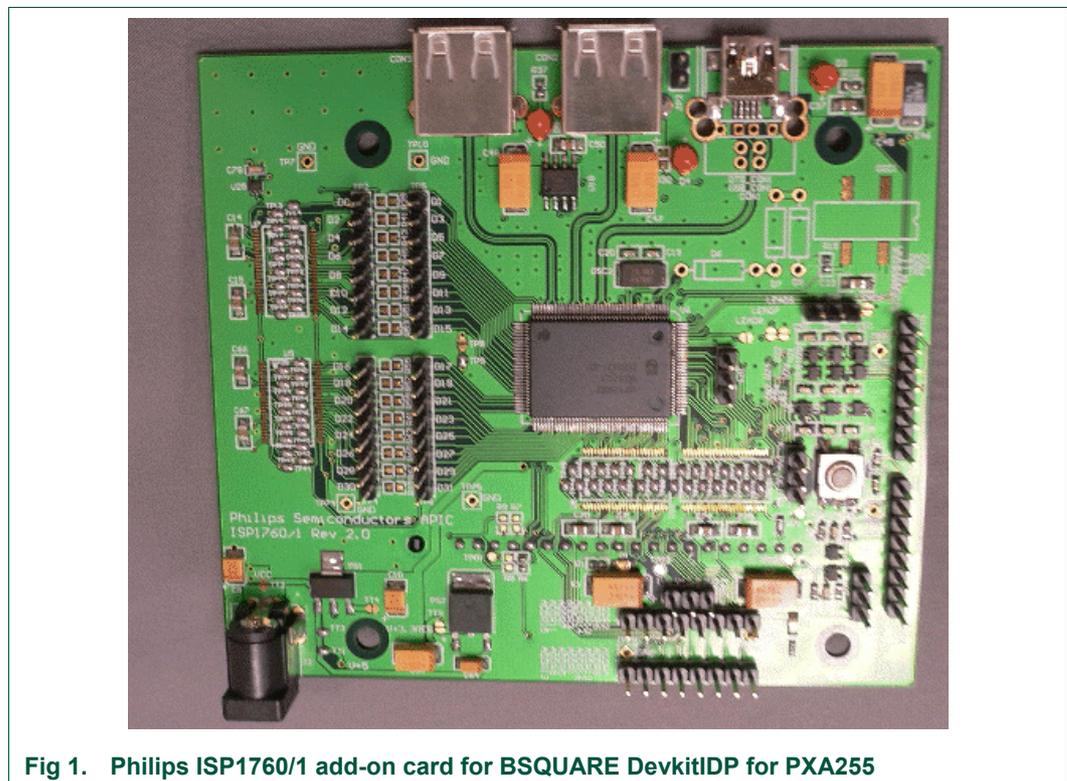


Fig 1. Philips ISP1760/1 add-on card for BSQUARE DevkitIDP for PXA255

## 2. ISP176x PXA255 eval board features

- Compatible with the BSQUARE DevkitIDP for PXA255 extension bus.
- Direct connection (minimal glue logic) to the BSQUARE DevkitIDP for PXA255 extension bus.
- Three USB ports: For the ISP1761, port 1 can be configured as a downstream, an upstream or an OTG port; ports 2 and 3 are always downstream ports; for the ISP1760, all three ports are downstream.
- 12 MHz crystal or oscillator options for the ISP176x input clock.

- Flexible choice of the HC\_IRQ and DC\_IRQ lines allocation to the PXA255 GPIO pins (J\_INT1).
- Optional configuration for analog or digital overcurrent protection. Both options are present on the PCB.
- All CPU interface signals are easily accessible on test headers designed for direct connection of a standard Tektronix logic analyzer.
- Flexible port 1 configuration with Type A, Type B and OTG mini-AB connectors. All options are present on the PCB.
- Jumper JINT2 for configuration of the ISP176x  $V_{CC(I/O)}$  power source from the BSQUARE DevkitIDP main board or from an external PSU (connected to TP50) provides possibility of using the 1.8 V power.
- Option to connect an external 3.3 V or 5.0 V source for the onboard voltage regulator input.
- Flexible configuration of  $V_{CC(5V0)}$ , the ISP176x power input. Either 3.3 V or 5.0 V can be used.

### 3. System requirements

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BSQUARE DevkitIDP for PXA255 development platform (hardware Ver. 4.0) running Linux Red Hat kernel Ver. 2.4.18 is required.

### 4. Jumper settings

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The ISP176x PXA255 eval board has the following jumper settings.

#### 4.1 J\_INT1

This is used to connect HC\_IRQ or DC\_IRQ to the PXA255 GPIO10 on the extension connector. HC\_IRQ and DC\_IRQ have default connections to certain PXA255 GPIO through optional resistors R4 and R5. For connections, see [Section 6](#).

- For 1 - 2: HC\_IRQ is connected to GPIO10.
- For 2 - 3: DC\_IRQ is connected to GPIO10.

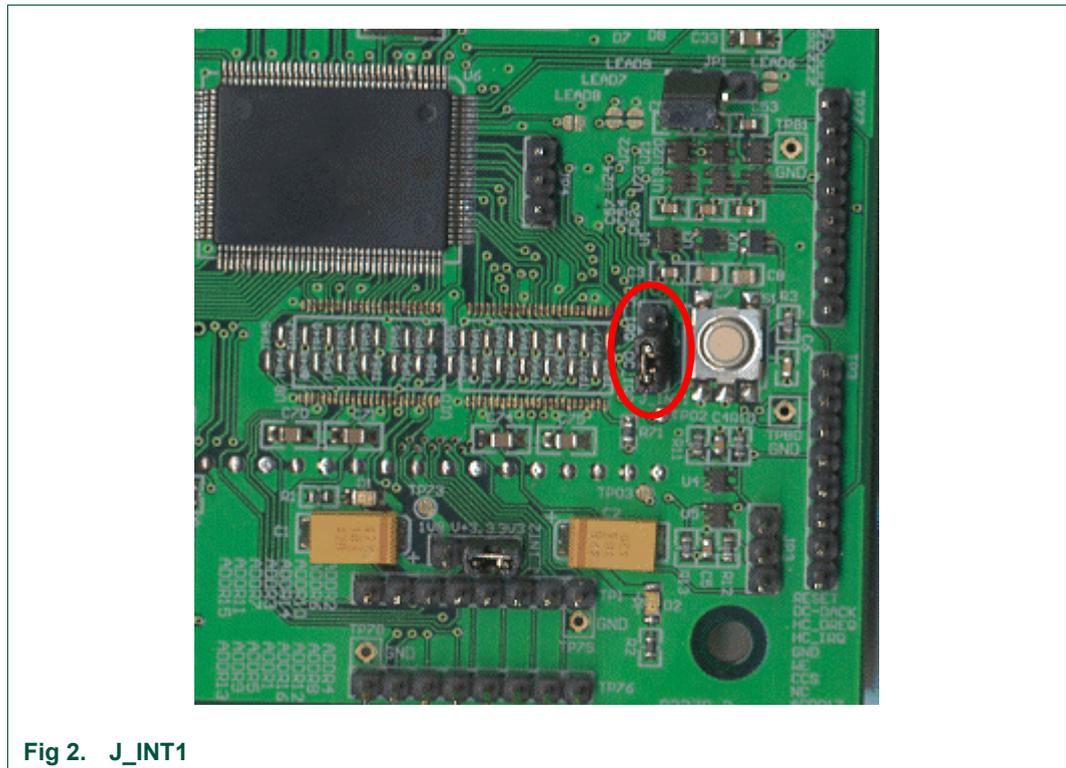


Fig 2. J\_INT1

## 4.2 J\_INT2

This jumper allows 3.3 V to be selected from the BSQUARE DevkitIDP internal power supplies or from an external power supply. Alternatively, a 1.8 V can also be connected using pad TP50.

- For 1 - 2: Default BSQUARE DevkitIDP 3.3 V power supply is selected.
- For 2 - 3: An external 3.3 V power source connected to TP50 can be used.



Fig 3. J\_INT2

## 4.3 JP1

This is used to test the ISP176x internal charge pump. The default normal connection must always be in position 2 - 3, which will connect  $V_{CP\_IN}$  to 3.3 V. Do not switch the jumper to position 1 - 2 because this does not ensure correct functionality of the charge pump.

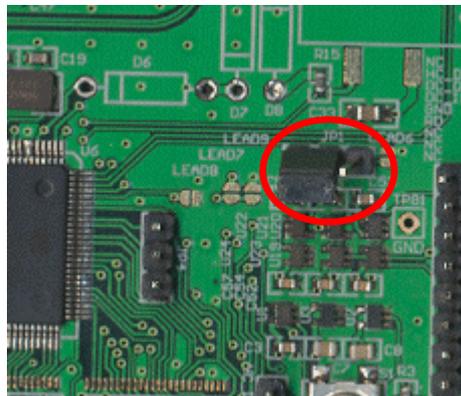


Fig 4. JP1

#### 4.4 Charge pump configuration

Do not connect LEAD6, LEAD7, LEAD8 and LEAD9. These must always remain open for correct functionality of the ISP176x. These are for test purposes only.

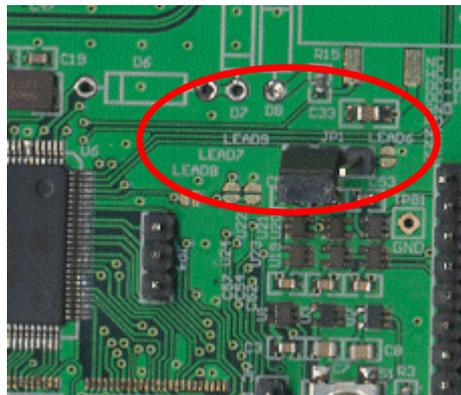


Fig 5. LEAD6, LEAD7, LEAD8 and LEAD9

#### 4.5 $V_{CC(5V)}$ input voltage selection

Connect or disconnect jumpers TT3 and TT4 to select the ISP176x input voltage.

When TT3 is soldered, the 5 V input to the ISP176x is selected. In this case, TT4 must be open.

When TT4 is soldered, the 3.3 V input to the ISP176x is selected. In this case, TT3 must be open.



Fig 6. TT3 and TT4

#### 4.6 Eval board input voltage selection

The input voltage to the eval board can be supplied from either the BSQUARE DevkitIDP 5 V power supply or an external power supply, by configuring TT1 and TT2.

When TT1 is soldered, the BSQUARE DevkitIDP 5 V power supply is used. In this case, TT2 must remain open.

When TT2 is soldered, an external power supply must be connected to J2. The external power supply must be: 5 V / 2 A. (Considering a maximum of 0.5 A on each USB port). In this case, TT1 must be open.

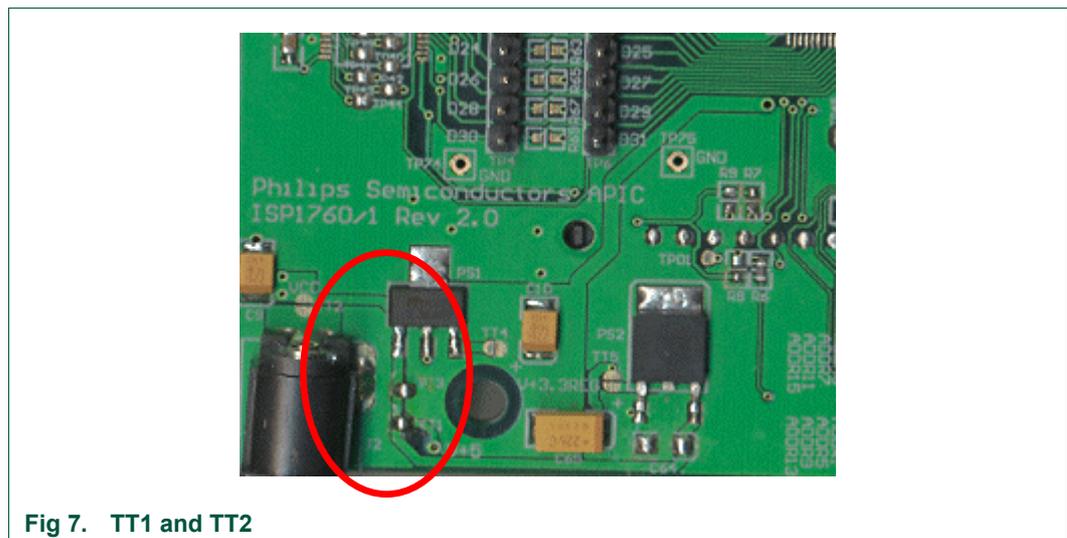


Fig 7. TT1 and TT2

## 5. ISP176x eval board schematics description

### 5.1 USB ports

The ISP1761 has three ports: Port 2 and port 3 are always configured as Host Controller ports, and port 1 can be connected to either the Host Controller or the Peripheral Controller.

The default connector soldered on port 1 is a Type B USB connector because port 1 will usually be used as a peripheral. Port 1 is, by default, routed to the Peripheral Controller

at start-up. The board also has options to solder a Type A or an OTG USB connector on port 1.

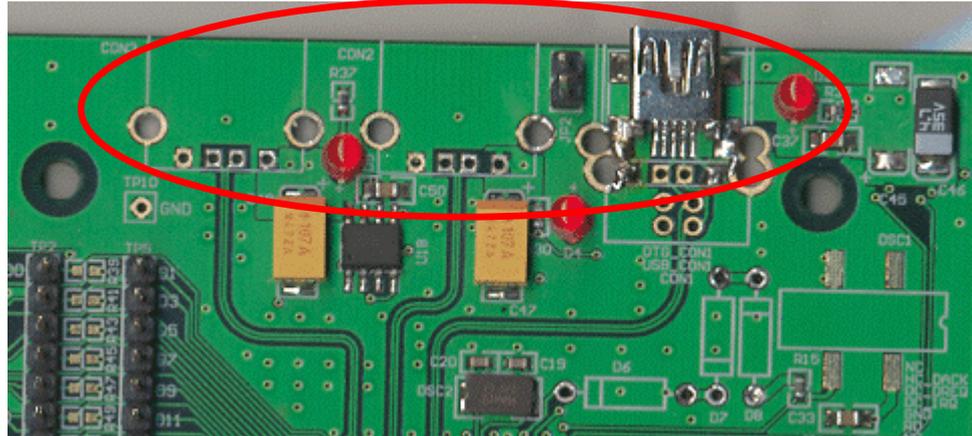


Fig 8. USB ports

## 5.2 LED indicators

There is a port power LED indicator for each port. Each LED will be on as soon as the port power of the respective port is enabled by software, for example, after loading drivers.

Port 1 power will not be enabled at start-up because port 1 is routed to the Peripheral Controller by default.

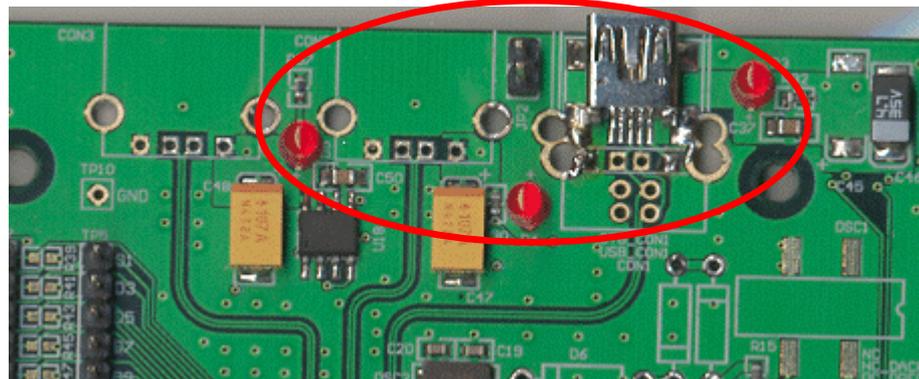


Fig 9. LED indicators

## 5.3 Port power switching and overcurrent detection circuit

The overcurrent detection circuit can be implemented using the digital or analog ISP176x internal detection circuit. The ISP176x eval board is designed for both options: either one can be soldered. By default, the digital overcurrent detection is implemented on port 2 and port 3, and the analog overcurrent detection is used on port 1.

**Remark:** The digital overcurrent protection on ports 2 and 3, and the analog overcurrent protection on port 1 cannot be simultaneously performed because there is only one bit for

the digital and analog overcurrent setting for all three ports. The reason for configuring the eval board for both digital and analog overcurrent is for flexibility of evaluation.

#### 5.4 Power sources and voltage regulator

A linear voltage regulator (3.3 V output) provides power for the ISP176x. The input to the regulator is voltage 5 V provided by the BSQUARE DevkitIDP board, by default jumpers' connections on the eval board.

Alternatively, an external power source can be connected to input jack J2, as described in [Section 4](#). The USB  $V_{BUS}$  voltage for USB ports is generated from the same voltage source; by default, the BSQUARE DevkitIDP 5 V source or an external power supply.

#### 5.5 CLK sources

The ISP176x clock source can be an external 12 MHz crystal or a 12 MHz oscillator. Both options are present on the eval board; selection is done by soldering correct components according to the ISP1760/1 data sheet.

#### 5.6 Test headers

Test headers allow you to connect a logic analyzer on all ISP176x CPU interface signals. U7, U8, U9 and U10 are optional level shifter ICs that allow evaluation of the ISP176x functionality with a 1.8 V bus.

## 6. Schematics

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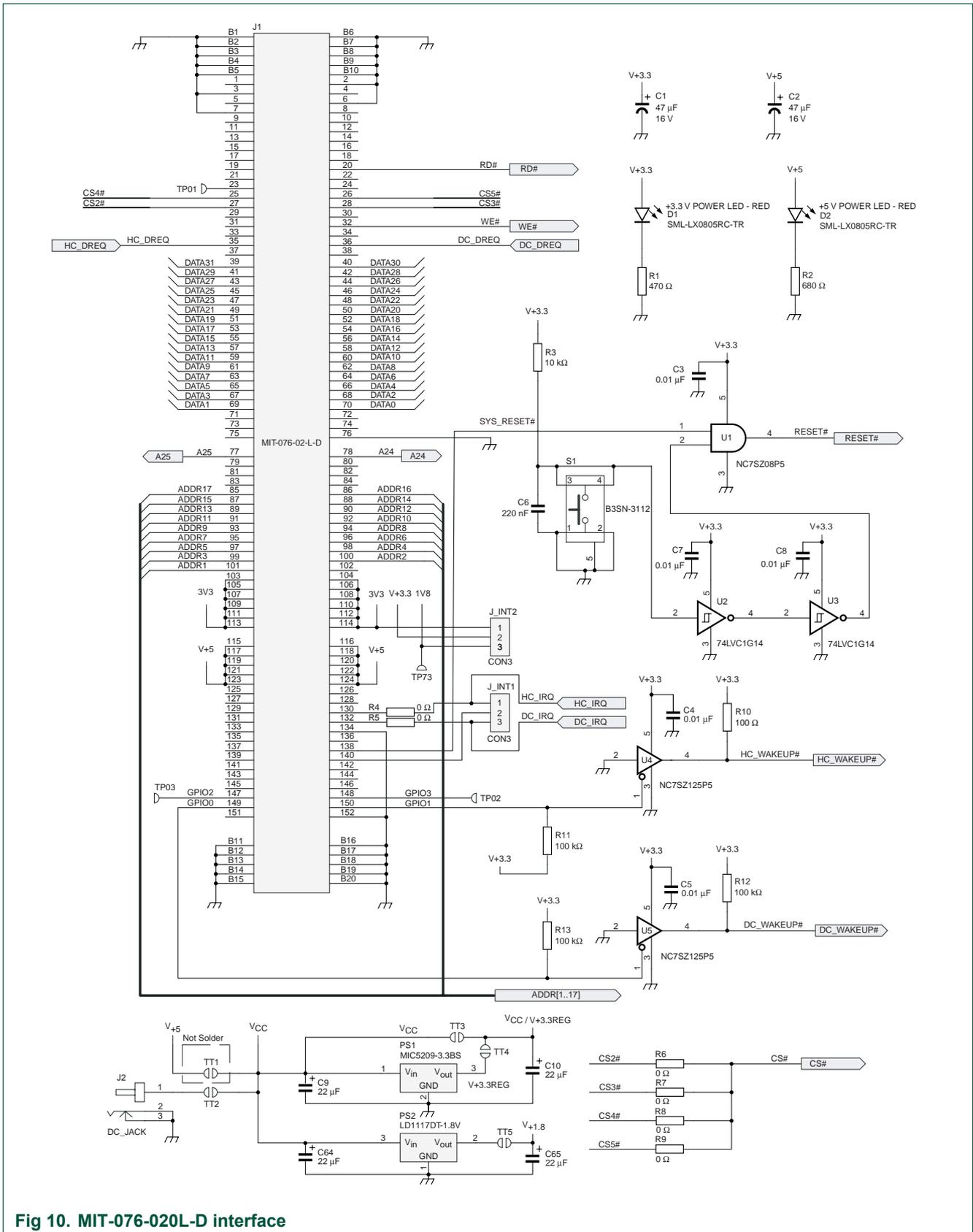


Fig 10. MIT-076-020L-D interface

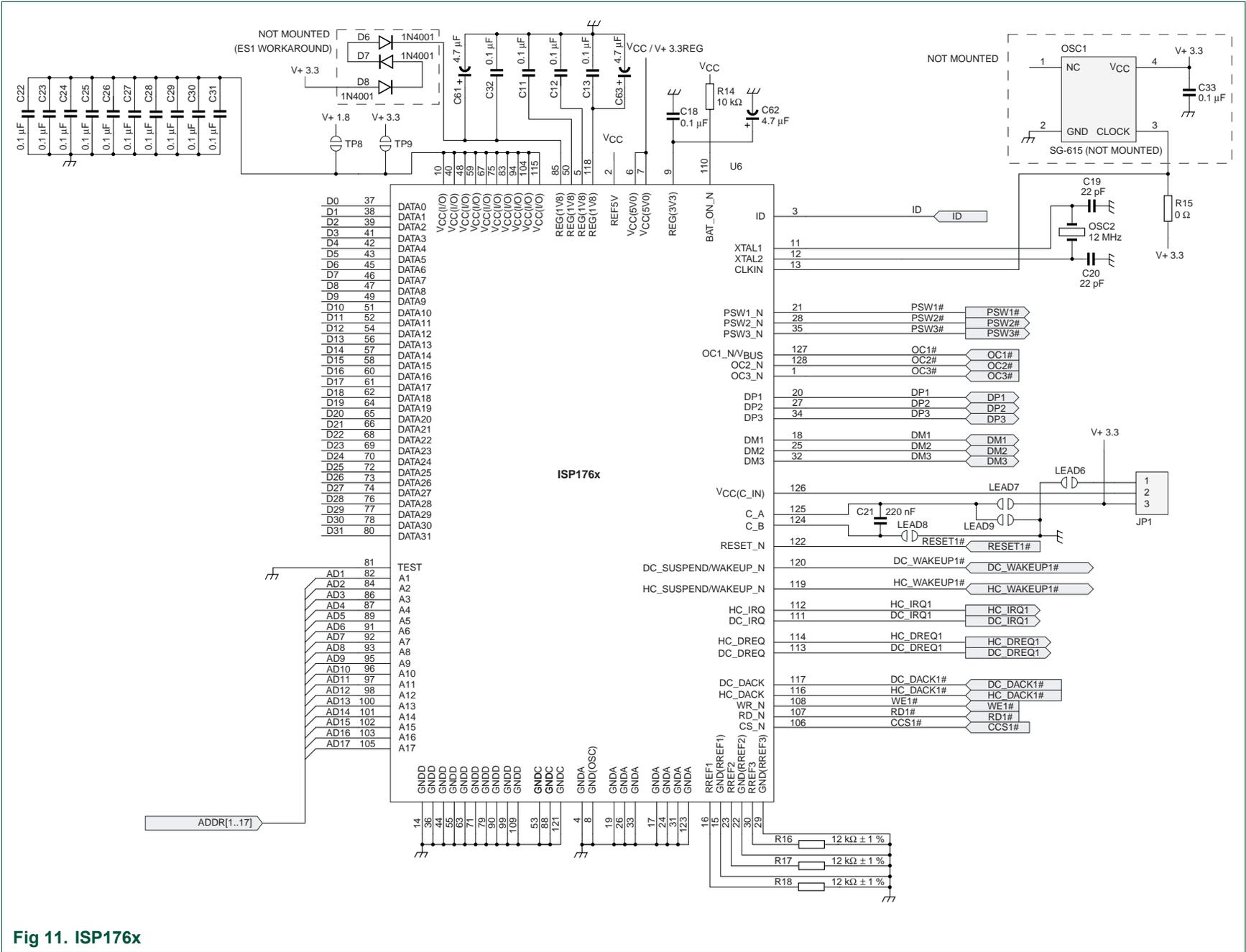


Fig 11. ISP176x



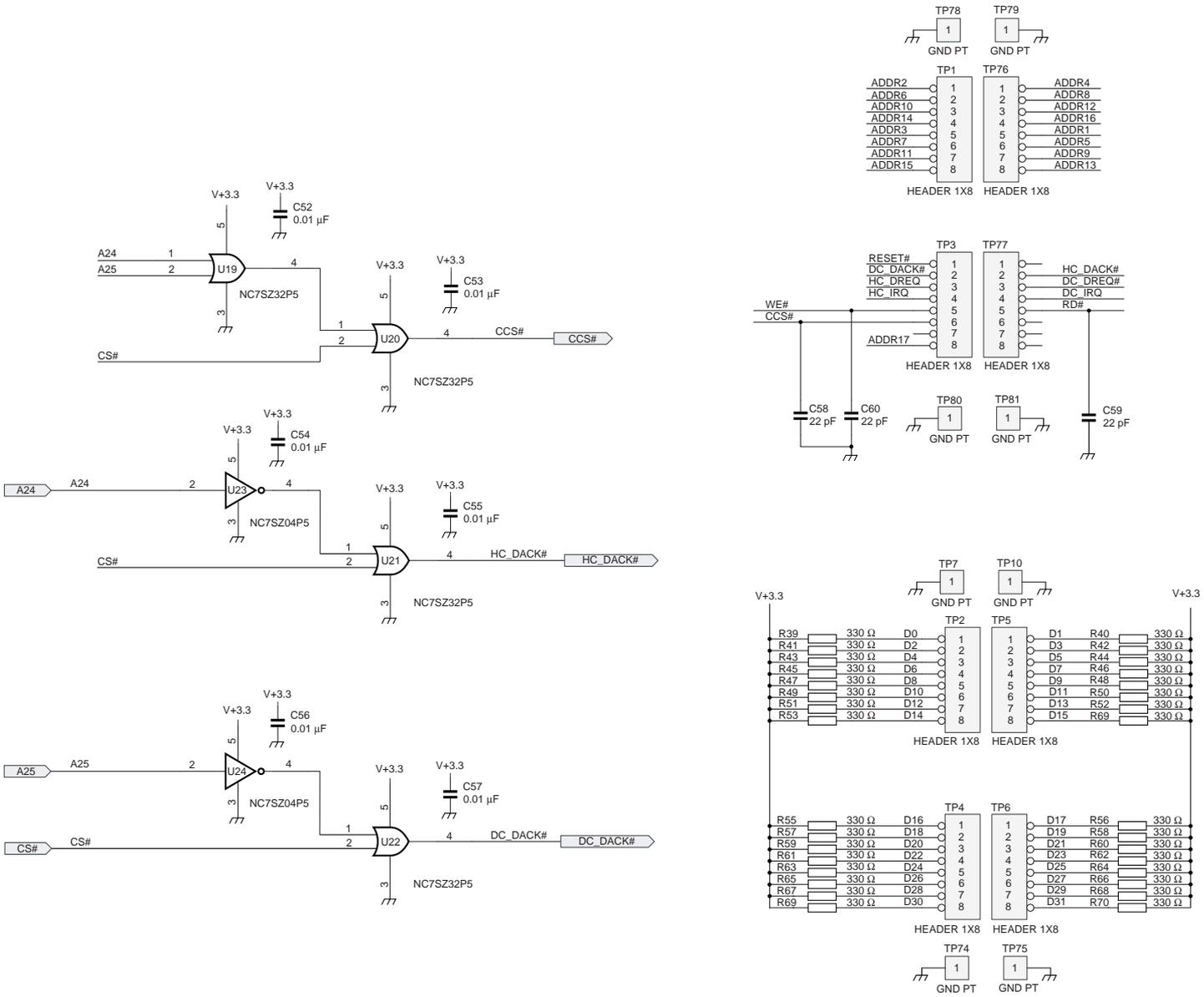


Fig 13. Logic circuit and pin header

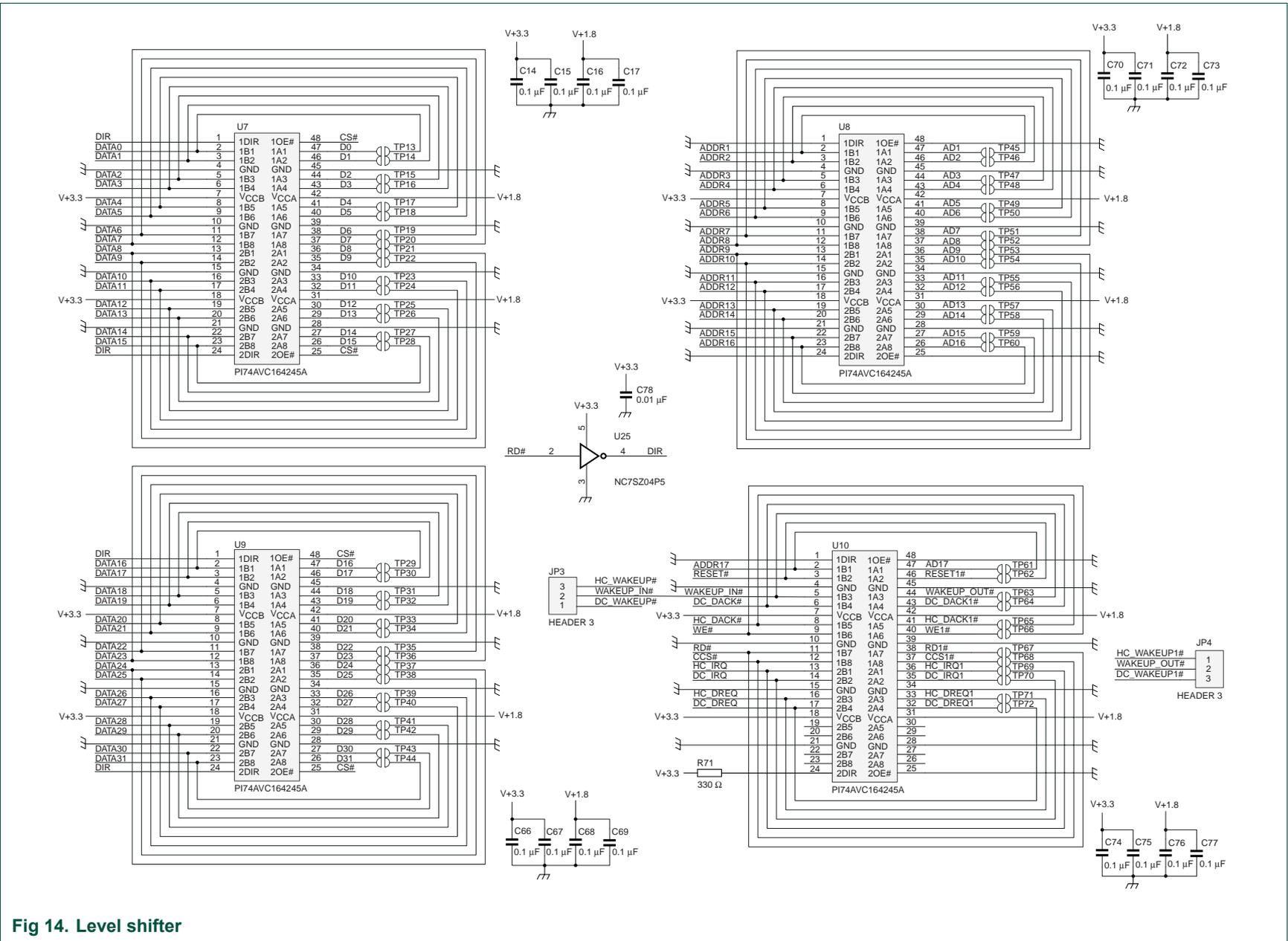


Fig 14. Level shifter

## 7. Bill of materials

Table 1: Bill of materials

Designator	Part Type	Footprint	Description
JP1	*	SIP3	Header, 3-pin
C54 C3 C57 C52 C53 C5 C78 C4 C56 C55	0.01 $\mu$ F	0603C	Capacitor
C17 C70 C15 C16 C66 C68 C69 C67 C72 C71 C75 C73 C74 C77 C76 C14	0.1 $\mu$ F	0805C	Capacitor (Semiconductor SIM Model)
C33 C51 C49 C50 C36	0.1 $\mu$ F	0805C	Capacitor
R9 R25 R30 R31 R5 R4 R6 R7 R8 R15	0 $\Omega$	0603R	Resistor 0603
D8 D7 D6	1N4001	1N4001	-
C62 C61 C63	4.7 $\mu$ F	CASE-A	Capacitor
R38	4.7 k $\Omega$	0603R	Resistor 0603
R24 R21 R20 R19 R14 R23 R22 R3	10 k $\Omega$	0603R	Resistor 0603
R17 R16 R18	12 k $\Omega$ 1 %	0603R	Resistor 0603
OSC2	12 MHz	12MHZ	Crystal Oscillator
C59 C60 C58	22 pF	0603C	Capacitor
C64	22 $\mu$ F	CASE-A	-
C65	22 $\mu$ F	CASE-C	-
C10 C9	22 $\mu$ F	SMD-B_22UF/16V	-
C2 C1	47 $\mu$ F	CASE-D	Capacitor
U2 U3	74LVC1G14	SOT353	Single Schmitt-trigger inverter
R10 R12 R11 R13	100 k $\Omega$	0603R	Resistor 0603
R34 R33 R32	100 $\Omega$	0603R	Resistor 0603
C45	100 $\mu$ F/25 V	100UF/10V	Polarized Capacitor (Axial)
R36 R37 R35	220 $\Omega$	0603R	Resistor 0603
R39 R45 R47 R71 R41 R43 R49 R52 R54 R64 R46 R48 R50 R66 R58 R60 R62 R68 R70 R56 R57 R59 R61 R51 R53 R55 R63 R40 R42 R44 R65 R67 R69	330 $\Omega$	0603R	Resistor 0603

Designator	Part Type	Footprint	Description
R1	470 $\Omega$	0603R	Resistor 0603
R2	680 $\Omega$	0603R	Resistor 0603
S1	B3SN-3112	B3SN-3112	-
J_INT2 J_INT1	CON3	SIP3	Connector
C6 C19 C7 C8 C20 C21	Cap	0603C	Capacitor
C44 C43 C37 C13 C40 C41 C11 C18 C12	Cap	0805C	Capacitor
C48 C47	Cap Pol2	100UF/10V	Polarized Capacitor (Axial)
C46	Cap Pol2	CASE-C	Polarized Capacitor (Axial)
C27 C26 C31 C30 C25 C24 C23 C29 C28 C22 C32	Cap Semi	0805C	Capacitor (Semiconductor SIM Model)
J2	DC_JACK	DCJACK	-
TP79 TP78 TP81 TP80 TP10 TP7 TP75 TP74	GND PT	HEADER	-
TP76 TP1 TP77 TP3 TP5 TP2 TP6 TP4	HEADER 1X8	HEADER_1X8	-
JP4 JP3	HEADER 3	SIP3	Header, 3-Pin
JP2	Header 2H	SIP2	Header, 2-Pin, Right Angle
U12 U11 U13	IP4059CX/LF	IP4059CX5	USB 2.0/USB-OTG Integrated ESD Protection
U6	ISP1760/1	ISP1760/1- LQFP128	-
PS2	LD1117DT-1.8V	TO-252	-
TP45 TP70 TP49 TP51 TP48 TP46 TP47 TP38 TP39 TP37 TP35 TP36 TP40 TP43 TP44 TP34 TP41 TP42 TP62 TP63 TP69 TP61 TP64 TP67 TP68 TP65 TP66 TP54 TP55 TP52 TP53 TP56 TP59 TP60 TP57 TP58 TP33 TP17 TP16 TP15 TP20 TP19 TP18 TP50 TP9 TP8 TP14 TP13 TP72 TP21 TP29 TP71 TP28 TP30 TP31 TP32 TP24 TP23 TP22 TP26 TP27 TP25	LEAD2	SOLDER_PAD	SOLDER PAD
D5 D4 D3	LED	3MM_LED	LIGHT EMITTING DIODE
U17 U18	MIC2026-2	SOP-8	-
PS1	MIC5209-3.3BS	SOT-223	Voltage Regulator

Designator	Part Type	Footprint	Description
J1	MIT-076-02-L-D	MIT-076-02-L-D	-
U23 U24	NC7SZ04P5	NC7SZ04P5	-
U25	NC7SZ04P5	SC70	-
U1	NC7SZ08P5	SC70	TinyLogic UHS 2-Input AND Gate
U20 U19 U21 U22	NC7SZ32P5	NC7SZ32P5	-
U5 U4	NC7SZ125P5	NC7SZ125P5	-
U16 U15 U14	NDS9430	SO-8	-
OTG_CON1	OTGSOCKET	USB_AB	-
U9 U8 U10 U7	PI74AVC164245A	TSSOP-A	16-Bit 1.8-2.5V to 3.3V Level Shifting Transceiver with 3-State Outputs
OSC1	SG-615	SG-615	-
D2 D1	SML-LX0805RC-TR	SMD_LED	LIGHT EMITTING DIODE
TT3 TT4 TT1 TT5 TT2	SOLDER_PAD	SOLDER_PAD	SOLDER PAD
CON1 CON3 CON2	USB_DOWN	USB_A	-
USB_CON1	USB_UP	USB_B	-

## 8. Abbreviations

**Table 2: Abbreviations**

Acronym	Description
OTG	On-The-Go
PCB	Printed-Circuit Board
PSU	Power Supply Unit
USB	Universal Serial Bus

## 9. References

- Universal Serial Bus Specification Rev. 2.0
- ISP1761 Hi-Speed Universal Serial Bus On-The-Go controller data sheet
- ISP1760 Hi-Speed Universal Serial Bus host controller for embedded applications data sheet.

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